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Optimal Low Power Deduction using Clock Gating

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Abstract:

The tremendous rise in demand for smartphones brings the need for power optimization. In this generation, as the technology node changes as generation progresses the urge to minimize power utilization increased. The study portrays the integration of additional sensor and control units over the silicon to source the dynamic power consumption.

The reduction in the technology node of the CMOS technology has continued to rise due the ever increase in the demand for greater performance devices with lower power consumption. To accept the challenge, the desire to implement newer and more optimization techniques at processor and system level has come into limelight.

Keywords: Power, logic gates, flip flop, clock tree synthesis, timing analysis

I. INTRODUCTION

The major concerning factor for the SOCs is heavily constrained by the increased count of transistors and the need to lower the battery power consumption. One strategic way of tuning the power is by introducing a sequential circuit into the necessary blocks that dynamically switches off the supply is known as clock gating. This leads to development of battery efficient and faster operating SoCs.

One of the primary requirements while designing any circuit is to understand how much power it would dissipate for its application beforehand. The power can be mainly branched into two forms, static and dynamic power. The best performance can be achieved by lowering voltage and frequency in short.

The silicon manufacturing companies have adversely scaled over the past few years to cater the rising demand for more production and better-quality devices with maximum throughput.

Reducing power consumption in very large scale integrated circuit (VLSI) design has become an interesting area of research. Most portable devices on the market are battery powered. These devices strictly limit current loss. Reducing the energy consumption of such devices significantly extends battery life.

Due to less development in battery technology, low-power design has become a more challenging area of research. Two types of current are consumed in a digital circuit. (1) static power and (2) dynamic power. Static power consists of power due to leakage currents, while dynamic power consists of capacitive switching power and short-circuit power. In a VLSI circuit, a clock signal is used to synchronize the active components.

Clock power is an important component of power mainly because the clock is supplied to most circuit blocks and the clock changes every cycle. Thus, the total clock power is an important component of the total power dissipation of a digital circuit. Clock scaling is a well-known way to reduce clock power. In a sequential circuit, the use of individual blocks depends on the application, not all blocks are used at the same time, which leads to the possibility of dynamic power reduction. Clock lock technology prevents the clock from stalling, which prevents power loss due to unnecessary charging and unused circuit discharge. Inserting a clock optionally stops the clock circuit for the part that is not doing an active calculation. Local clocks that are conditionally enabled are called gates because the environmental signal is used to gate the global clock signal.

This paper reviews major architectural optimizations developed in recent times for significant reduction of batter power consumed using clocks.

II. DESIGN FOR CLOCK GATING

Clock gating is one of the convenient methods to reduce the switching factor of the dynamic power without impacting the efficiency of the functioning of the SoC. Effectively, the switching factor of the dynamic power can be lower to almost negligent by turn the clock off to the certain parts of the circuit. This idea can be implemented using basic logic gates or latches. The main intent of this type of clock gating is to enable the operation by modifying the logic of RTL.

A. Clock Gating using Gates

The simplest form of achieving timing and low power design is by using AND gate logic.

A combinational logic inputs the clock enable signal which in turn controls the entire activity of the downstream logic. If the enable signal has an input of 1, the clock will be passed on the flipflop and the other way round, if the input of the clock enable is 0, then the clock will be off and hence the activity of the flipflop will also be shut.

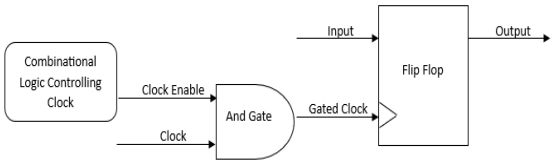

Figure 1: Clock Gating with AND Gate Logic.

But the easiest way mostly generates glitches in the gated clock with is given as the input to the flip flop, such glitches are undesirable.

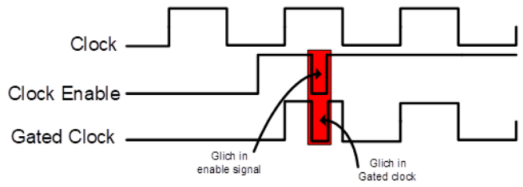

Figure 2: Glitches seen in Gated Clock

Another way of implementing is by using NOR gate logic, where the gated clock is high only when both clock enable and clock.

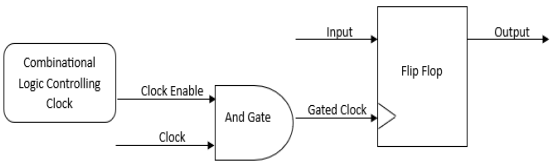

Figure 3: Clock Gating with NOR Gate Logic.

B. Clock Gating using Latch

Furthermore, the above-mentioned glitches can also be eliminated by using a negative edge triggered flip flop. This is also a latch that is low level sensitive at the output of the combinational logic.

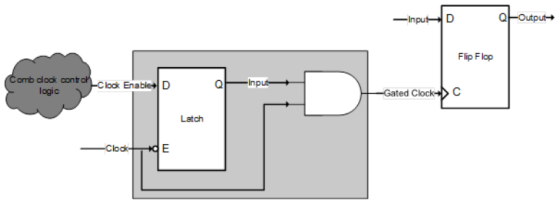

Figure 4: Clock Gating with Latch.

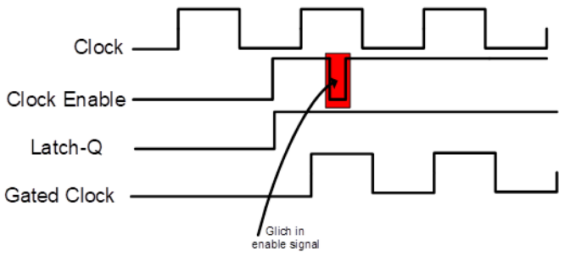

Figure 5: Gated Clock without any Glitches

The negative triggered latch, as the name says is provoked only during the negative clock cycle. Hence, the input to the AND gate in the Logic cell shown below would be stable when it's high.

C. Clock Gating Design based on D Flip Flop

The D flip flop is the only flip flop whose input is same as the output based on the edge of the clock. It also

serves its purpose as a memory storage unit as it ensures both the inputs are never equal to 1 at once.

For a positive edge triggered D flip flop, until the next positive trigger of the clock, the output is still held onto its value. Once, the positive edge of the clock is provoked the output replaces its current value with the value of the input and holds it till the next cycle. On the contrary for a negative edge triggered D flip flop, the output only changes in synchronous with the negative edge of the clock. But there does exist idle clock cycles where the output doesn't vary irrespective of the clock cycle, to avoid such situations an XOR logic is added, and its output is passed into the AND gate along the clock input.

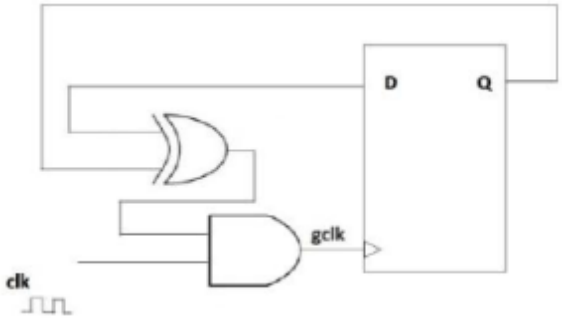

Figure 6: Clock Gating using D Flip Flop

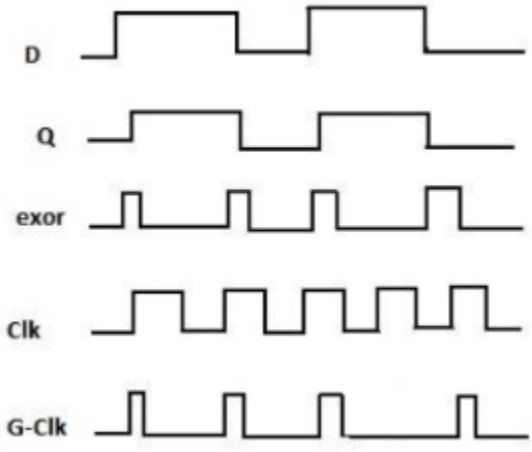

Figure 7: Gated D Flip Flop Waveform

The gated clock input to the D flip flop is attained because of the output of the AND gate, whose inputs are output of the EXOR gate and clock. The duty cycle of the gated clock is different from that of the input clock. Hence the output of the D flipflop varies based upon the edge of the gated clock than the actual clock fed into the system.

This technique helps shut off the combinational circuit that branches from here thereby showing a major impact in the reduction of power.

D. Clock Gating Using Global Enable

The introduction of global enable signal increases the complexity of the design and certain parameters like clock skew and jitter would come into play. The clock tree synthesis should be determined to minimize the skews and maintain balance amongst all the clock paths which are not a part of the clock gate circuit too. Another major impact would be on the setup and hold timings, static timing analysis would help in minimizing these factors.

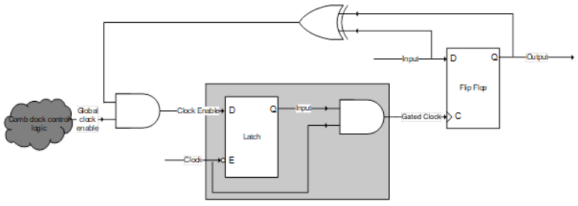

Figure 8: Clock Gating using Global Enable Signal

III. POWER ANALYSIS FOR CLOCK GATING

Generally, Xilinix tool is used to determine the power for any block in the circuit based on it Verilog code, how it is coded based on its behavioral model. Further, before even determining the power, the code needs to be simulated and checked for its working using a tool called MODELSIM.

Most frequently D flip flop is used for clock gating due to reduction in duty cycle of the gated clock. This will benefit the design by reducing the power consumed at a price of the area of design the D flip flop.

The primary reduction in power consumption can be calculated by feeding both the designs with and without clock gating into the Xilinix setup post MODELSIM simulation.

IV. PROS AND CONS OF USING CLOCK GATING

A well-designed clock gating circuit will maximum reduction of power benefits the designers to propose

low power budgets and provide scope for modifications of design during the initial phase.

Clock gating has proved to be efficient resulting in reduction up to 20% - 30% of the total dynamic power.

Clock benefits the dynamic power leaving the scope for improvements in the static power when dealt with smaller tech nodes.

The major drawback of clock gating is that it comes to a benefit with cost of the area and the increase in the clock complexity.

V. CONCLUSION

Clock gating optimization can be used in various systems like multi core CPUs, GPU and various FPGA circuits as well. This method is proven to achieve optimal power deductions without significant reduction in the performance of the design, with a little area overhead. The design proposed is compatible with most of the logic designs and can be implemented using various clock grid designs.

VI. REFERENCES

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